Amendments to the Claims

1. (Original) A bridge controller for transferring data between a data storage device and a data utilization device, the bridge controller receiving a command information packet for controlling the data transfer, comprising:

a state machine receiving command information in a background mode in real time as the packet is being transferred to the bridge controller, the state machine utilizing the command information to set up the receiving device for the data transfer; and

a programmable processor coupled to the command information packet after the packet has been received, the processor making changes to the set up of the receiving device for the transfer, if needed, and then initiating the data transfer.

2. (Currently Amended) The bridge controller of Claim 1 wherein the command information packet is received serially from the [date] data utilization device.

3. (Original) The bridge controller of Claim 1 wherein the command information packet is stored in a buffer memory in the bridge controller.

4. (Original) The bridge controller of Claim 3 wherein the information of the command information packet is processed in real time by the state machine as it is being stored in the buffer memory.

5. (Original) The bridge controller of Claim 4 wherein the buffer memory is a first in first out (FIFO) buffer memory.

6. (Original) The bridge controller of Claim 4 wherein the processor is interrupted once the buffer memory is full.

7. (Original) The bridge controller of Claim 1 wherein the data utilization device is a computer and the data storage device is an ATA or ATAPI device.

8. (Currently Amended) The bridge controller of Claim 7 wherein the link between [the] a bridge and the computer is by a Universal Serial Bus (USB) link.

9. (Original)The bridge controller of Claim 7 wherein the data storage device is a device selected from the group consisting of an ATA hard drive, an ATAPI CD drive or an ATAPI DVD drive, Compact Flash Card, or MO drive.

10. (Original) The bridge controller of Claim 1 wherein the state machine is formed in an ASIC.

11. (Original) A USB to ATA/ATAPI bridge comprising:

a physical layer receiving serial command data from the USB bus and converting the data to a parallel format;

a transfer controller receiving the parallel data for transferring the data to a buffer memory;

a state machine operating in background mode on the parallel data flowing through the transfer controller in real time to set up the ATA or ATAPI device for a data transfer; and

a programmable processor coupled to the buffer memory and being interrupted after all command information has been received, to individually alter any set up data for the ATA or ATAPI device that is needed, and then initiating the data transfer.

12. (Original) The bridge of Claim 11 wherein the serial data is on a USB 2.0 bus.

13. (Original) The bridge of Claim 12 wherein the serial data is from a USB host in a computer.

14. (Original) The bridge of Claim 11 wherein the command data is in the form of a command block wrapper (CBW).

15. (Original) The bridge of Claim 11 wherein the ATA device is an ATA hard drive and the ATAPI device is an ATAPI CD drive or an ATAPI DVD drive.

16. (Original) The bridge of Claim 11 further comprising a plurality of task registers in the bridge receiving command data, the registers containing data needed by the ATA or ATAPI device to set up a data transfer.

17. (Original) The bridge of Claim16 wherein the processor transfers data in the plurality of registers to the ATA or ATAPI device to prepare for data transfer.

18. (Original) The bridge of Claim 11 wherein the state machine is formed in an ASIC.

19. (Original) A method of operating a USB to ATA or ATAPI bridge comprising:

transferring command data from a data utilization device via a USB bus through a data transfer device to a buffer memory;

operating a state machine in a background mode using data flowing through the data transfer device in real time to extract set up data and store the data to set up a data transfer;

operating a programmable processor utilizing the data stored in the buffer memory to individually alter the command-related data for the ATA or ATAPI device that is needed; and

initiating the data transfer.

20. (Original) The method of Claim 19 wherein the command data is a command block wrapper (CBW) for a USB 2.0 mass storage class protocol, the set up data is transferred to a plurality of registers in the bridge and is then transferred to the ATA or ATAPI device before the data transfer commences.